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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/727,393	11/29/2000	Allen P. Chen	10559-385001/P10191	4146

20985 7590 07/17/2006

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EXAMINER	
SEFCHECK, GREGORY B	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 07/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/727,393	CHEN ET AL.	
	Examiner	Art Unit	
	Gregory B. Sefcheck	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 13-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 13-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

- Applicant's Amendment filed 5/11/2006 is acknowledged.
- Claim 42 has been amended.
- The previous rejection of claim 42 under 35 USC 112, 2nd paragraph is withdrawn in light of the present amendment.
- Claim 12 had been previously cancelled.
- Claims 1-11 and 13-42 are pending.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 6, 7, 9-11, 13, 15, 16, 18, 19, 24, 26-33, 35-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cam et al. (US006671758B1), hereafter Cam, in view of Bucholz et al. (US005440545A), hereafter Bucholz.

- In regards to Claims 1, 2, 4, 6, 9, 10, 13, 15, 16, 18, 19, 24, 26-28, 32, 35-41, Cam discloses a packet data transfer method on an interface having a large number of ports (Abstract; claim 1,9,24 – intra-packet switching).

Referring to Fig. Cam shows that a Layer/master device 22 polls the PHY devices 14-20 to determine which have data waiting to be transferred (Col. 1, lines 38-

41; claim 1,9,24,32 – determining which ports contain a data packet available for processing).

Cam shows that data packets waiting to be transferred from polled PHY devices are fragmented to a maximum block size (cell) of data. This maximum block size may be fixed at start-up or by programming through an external management interface (Col. 3, lines 2-9; claim 1,9,24,32 – fragmenting available data packet into at least one cell having defined size; claim 1,9,24,26,32 – fragmentation continues until a user-defined number of cells are generated; claim 2,10,27 – monitoring the number of cells produced to determine if user-defined number are generated; claim 18,19 – user interface for allowing user to specify user-defined cells to be generated by packet fragmentation process).

Referring to Figs. 5, 6, and 11, Cam shows that packets awaiting transfer from multiple PHY devices will be transferred a maximum block size at a time before deselecting itself, at which point the next PHY device begins transfer of a maximum block size. As such, a first selected PHY device having a first packet to be transferred that is greater than the maximum block size (i.e. 256 bytes; Col. 3, lines 6-7) will fragment and transmit a first portion of the packet during a first transfer period. The selected PHY is deselected after transmission of the maximum block size, a subsequent PHY device is selected and packet fragmentation and transmission is repeated for that newly-selected PHY device, up to the maximum block size per transfer period. The remaining portions of the first packet at the first PHY device will be fragmented and transferred during the next selected transfer period, after all other PHY devices have

been given a chance to transmit (Col. 3, lines 6-7 and line 55-Col. 4, line 24; claim 1,9,24,26,32 - fragmenting a first portion of a second available data packet on a different port subsequent to fragmenting a first portion of the first data packet but prior to fragmenting a second portion of the first available data packet; claim 40 – user-defined number of cells comprises at least 2 cells).

Cam does not explicitly disclose fragmentation of the first available packet using a signal processing circuit and storing, in memory of the processing circuit, a data element indicative of the incomplete fragmentation status concerning the first available packet, comprising a data packet length remainder indicative of the packet portion not fragmented and a packet truncation indicator indicative of incomplete fragmentation of the packet, if another port contains an available packet, where the element allows subsequent processing of the remainder of the data packet, after subsequent fragmentation of a second packet.

Bucholz discloses a packet delivery system in which packets are fragmented for transmission (Title; Abstract). Referring to Fig. 6, Bucholz shows that a reassembly header (stored data element) is stored in the fragmented packet indicating its place within the packet, total packet length, total fragments, etc. such that the progress of the packet's fragmentation can be determined (Col. 6-7, lines 63-23; claim 1,4,9,24,32 – storing, in memory, data element indicative of the incomplete fragmentation status concerning the packet being processed if another port contains an available packet, where the element allows subsequent process of the remainder of the data packet

being processed; claim 13,35,37 – data packet length remainder indicative of packet portion not fragmented; claim 13 – packet truncation indicator indicative of incomplete fragmentation of the packet; claim 6,15,16,28 – monitoring and determining if the data packet has been fully fragmented; claim 36 – indicator indicative of the length of a packet previously fragmented; claim 36,37 - indicator indicative of total length of packet; claim 38 – fragmenting a second portion of the first packet subsequent to fragmenting a first portion of a second packet; claim 39 – using the stored data element to enable fragmenting the second portion of the first packet).

Referring to Figs. 1b and 2, Bucholz discloses that packet fragmentation is performed in a packet switching device 100 that comprises a processor 110 (signal processing circuit) and associated memory 232 for storing the reassembly header (claim 41 - fragmentation of the first available packet using a signal processing circuit; claim 41 – storing data element concerning the first available packet in memory of the processing circuit).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Cam by processing packet fragments in a signal processing circuit and storing a reassembly header for a first packet being processed in memory of the processing circuit, the header including information regarding total packet length, how much of the packet has been fragmented and how much remains to be fragmented, so that subsequent fragment processing of other packets and the remainder of the first packet can be performed, as taught by Bucholz. This would enable determination of when packet fragmentation of a large packet transmitted in

multiple fragments has been completed, as well as enable the transmission system of Cam to recognize the progress and status of packet fragmentation so that packets need not be completely fragmented before the per-device polling mechanism proceeds to processing of packets at other PHY devices.

- In regards to Claims 3 and 11,

Cam discloses a packet data transfer process that covers all limitations of the parent claim.

Referring to Fig. 5, Cam shows that polling of the PHY devices to determine if packets are available for processing is continuously done so that it is determined if any other ports contain packets available for processing other than those that have already so indicated (Col. 1, lines 38-41; Col. 3, lines 19-24; claim 3,11 – re-determining if packets are available for processing on any of the plurality of ports if the number of cells have been generated from the first port determined to have a packet available).

- In regards to Claim 7,

Cam discloses a packet data transfer process that covers all limitations of the parent claim.

Referring to Fig. 5, Cam shows that polling of the PHY devices to determine if packets are available for processing is continuously done so that it is determined if any other ports contain packets available for processing other than those that have already so indicated (Col. 1, lines 38-41; Col. 3, lines 19-24; claim 7 – re-determining if packets

are available for processing on any of the plurality of ports if the number of cells have been generated from the first port determined to have a packet available).

- In regards to Claims 29-31 and 33,

Cam discloses a packet data transfer process that covers all limitations of claim 29 similar to claims 1, 9, 24, and 32 as shown above.

Cam does not explicitly show implementing the methods and processes through computer programs residing on computer readable medium such as read-only and random access memory in which the processor and memory are on a single board computer.

It is well known that software implementation by a computer having a processor and memory for performing process/method functions can be cost efficient and enable accessibility for updates/upgrades of the processes to accommodate new technologies (claim 29 – computer program product residing on computer readable medium; claim 30 – computer readable medium is ROM; claim 31 - computer readable medium is RAM; claim 33 – processor and memory are incorporated into single board computer).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the method of Cam through a processor running software from a read-only or random access memory in a single board computer. Implementations of methods and processes through software instructions residing on computer readable medium such as ROM and RAM can be much less expensive than hardware

implementations and provide accessibility for updates/upgrades of the processes to accommodate new technologies.

- In regards to Claim 42,

Cam discloses a packet data transfer method on an interface having a large number of ports (Abstract; claim 42 – programmable intra-packet switching method).

Referring to Fig. Cam shows that a Layer/master device 22 polls the PHY devices 14-20 to determine which have data waiting to be transferred (Col. 1, lines 38-41; claim 42 – determining which ports contain a data packet available for processing).

Cam shows that data packets waiting to be transferred from polled PHY devices are fragmented to a maximum block size (cell) of data. This maximum block size may be fixed at start-up or by programming through an external management interface (Col. 3, lines 2-9; claim 42 – fragmenting available data packet into at least one cell having defined size; claim 42 – fragmentation continues until a user-defined number of cells are generated; claim 42 – monitoring the number of cells produced to determine if user-defined number are generated).

Referring to Figs. 5, 6, and 11, Cam shows that packets awaiting transfer from multiple PHY devices will be transferred a maximum block size at a time before deselecting itself, at which point the next PHY device begins transfer of a maximum block size. As such, a first selected PHY device having a first packet to be transferred that is greater than the maximum block size (i.e. 256 bytes; Col. 3, lines 6-7) will fragment and transmit a first portion of the packet during a first transfer period. The

selected PHY is deselected after transmission of the maximum block size, a subsequent PHY device is selected and packet fragmentation and transmission is repeated for that newly-selected PHY device, up to the maximum block size per transfer period. The remaining portions of the first packet at the first PHY device will be fragmented and transferred during the next selected transfer period, after all other PHY devices have been given a chance to transmit (Col. 3, lines 6-7 and line 55-Col. 4, line 24; claim 42 – re-determining which ports contain a data packet available for processing if the user defined number of cells have been generated; claim 42 - fragmenting a first portion of a second available data packet on a different port subsequent to fragmenting a first portion of the first data packet but prior to fragmenting a second portion of the first available data packet).

Cam does not explicitly disclose storing, in memory, a data element including a first data element indicative of the incomplete fragmentation status concerning the first available packet and a second data element indicative of the packet portion not fragmented or remaining to be fragmented, if another port contains an available packet, where the data element allows subsequent processing of the remainder of the data packet, after subsequent fragmentation of a second packet on a different port.

Bucholz discloses a packet delivery system in which packets are fragmented for transmission (Title; Abstract). Referring to Fig. 6, Bucholz shows that a reassembly header (stored data element) is stored in the fragmented packet indicating its place within the packet, total packet length, total fragments, etc. such that the progress of the

packet's fragmentation can be determined (Col. 6-7, lines 63-23; claim 42 – storing, in memory, data element indicative of the incomplete fragmentation status concerning the packet being processed if another port contains an available packet, where the element enables subsequent process of the remainder of the data packet being processed; claim 42 – second data element indicative of packet portion not fragmented or length of a packet previously fragmented; claim 42 – data element enables fragmenting a second portion of the first packet subsequent to fragmenting a first portion of a second packet on a different port).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Cam by processing packet fragments and storing a reassembly header for a first packet being processed including information regarding incomplete fragmentation status of the packet and either how much of the packet has been fragmented or how much remains to be fragmented, so that subsequent fragment processing of other packets on different ports as well as the remainder of the first packet can be performed, as taught by Bucholz. This would enable determination of when packet fragmentation of a large packet transmitted in multiple fragments has been completed, as well as enable the transmission system of Cam to recognize the progress and status of packet fragmentation so that packets need not be completely fragmented before the per-device polling mechanism proceeds to processing of packets at other PHY devices.

3. Claims 5, 8, 14, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cam in view of Bucholz as applied to claims 4, 7, 11, and 16 above, and further in view of Colmant et al. (US006144662A).

- In regards to Claims 5, 8, 14, and 17,

Cam discloses a packet data transfer process that covers all limitations of the parent claim.

Cam does not explicitly show initiating fragmentation on a data packet from another port while the fragmentation of the data packet on the first port continues until user-defined cells are generated.

Colmant discloses a non-blocking switch. Referring to Figs. 1B and 3B, Colmant shows that a packet received on a port 85 may be fragmented into several portions (6001-6004) while another received packet on another port 85 is fragmented into portions (6125-6128), thereby enabling multiple port packet fragmentations to operate in parallel, thereby improving the utilization of the transmission medium and keeping waiting time for a blocked output port low (Col. 9, lines 14-42; claim 5,8,14,17 – initiating fragmentation on a data packet from another port while the fragmentation of the data packet on the first port continues until user-defined cells are generated).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Cam to enable a received packet on another port proceed with fragmentation while the fragmentation of a first packet on the first port

continues. By fragmenting received packets in parallel, processing delay required to fragment a packet prior to transmission could be eliminated.

4. Claims 20-23 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cam in view of Bucholz, as applied to claims 9 and 32 above, and further in view of Jha (US006847644B1).

- In regards to Claims 20-22 and 34,

Cam discloses a packet data transfer method on an interface having a large number of ports that covers all limitations of parent claim 9. (Abstract).

Referring to Fig. Cam shows that a Layer/master device 22 polls the PHY devices 14-20 to determine which have data waiting to be transferred (Col. 1, lines 38-41; claim 21 – determining which ports contain a data packet available for processing).

Cam shows that data packets waiting to be transferred from polled PHY devices are fragmented to a maximum block size (cell) of data. This maximum block size may be fixed at start-up or by programming through an external management interface (Col. 3, lines 2-9; claim 21 – fragmenting available data packet into at least one cell having defined size; claim 21 – fragmentation continues until a user-defined number of cells are generated; claim 22 – monitoring the number of cells produced to determine if user-defined number are generated).

Referring to Figs. 5, 6, and 11, Cam shows that packets awaiting transfer from multiple PHY devices will be transferred a maximum block size at a time before

deselecting itself, at which point the next PHY device begins transfer of a maximum block size. As such, a first selected PHY device having a first packet to be transferred that is greater than the maximum block size (i.e. 256 bytes; Col. 3, lines 6-7) will fragment and transmit a first portion of the packet during a first transfer period. The selected PHY is deselected after transmission of the maximum block size, a subsequent PHY device is selected and packet fragmentation and transmission is repeated for that newly-selected PHY device, up to the maximum block size per transfer period. The remaining portions of the first packet at the first PHY device will be fragmented and transferred during the next selected transfer period, after all other PHY devices have been given a chance to transmit (Col. 3, lines 6-7 and line 55-Col. 4, line 24; claim 21 - fragmenting a first portion of a second available data packet on a different port subsequent to fragmenting a first portion of the first data packet but prior to fragmenting a second portion of the first available data packet).

Cam does not explicitly show the plurality of ports connected to a synchronous optical network and the fragmentation process producing ATM cells. Cam also does not explicitly show a processor and memory of an ATM/POS processor for performing the method.

Jha discloses hybrid data transport over optical networks. Referring to Fig. 2 and 4, a switch's ports are connected to a SONET network. Jha shows that SONET data frames may be inverse-multiplexed (fragmented) into smaller bandwidth streams, such as ATM cell streams (Col. 1-2, lines 58-6; claim 21 - plurality of ports connected to a synchronous optical network; claim 20,21 - fragmentation process producing ATM

cells). Referring to Fig. 3, Jha also shows that processing of ATM and Packet-over-SONET can be accommodated through a single switch 102a/n (claim 34 – processor and memory are incorporated into ATM/POS processor).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the method of Cam through an ATM/POS processor such that the plurality of ports are connected to a SONET network and the fragmentation process produces ATM cells, as shown by Jha. This would enable the high bandwidth SONET frames to transport Ethernet over ATM using standard protocols, as shown by Jha (Fig. 2; Col. 2, lines 35-41).

- In regards to Claim 23,

Cam discloses a packet data transfer process that covers all limitations of the parent claim.

Cam does not explicitly show monitoring and determining if the data packet has been fully fragmented.

Bucholz discloses a packet delivery system in which packets are fragmented for transmission (Title; Abstract). Referring to Fig. 6, Bucholz shows that a reassembly header is stored in the fragmented packet indicating its place within the packet, total packet length, total fragments, etc. such that it can be determined when the packet is fully fragmented (Col. 6-7, lines 63-23; claim 23 – monitoring and determining if the data packet has been fully fragmented).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Cam by storing a reassembly header for the packet currently being processed, including information regarding how much of the packet has been fragmented and how much remains, so that subsequent processing of the remainder of the packet fragments can be performed, as taught by Bucholz. This would enable the transmission system to recognize when a complete packet has been processed when transmitted in a number of fragments.

5. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cam in view of Bucholz as applied to claim 24 above, and further in view of Muller et al. (US006105122A), hereafter Muller.

- In regards to Claim 25,

Cam discloses a packet data transfer process that covers all limitations of the parent claim.

Cam shows that PHY device addresses may be segmented to achieve balance between efficient memory mapping and address decoding. Cam does not explicitly disclose an unbalanced port-loading condition as a port-switching event.

Muller discloses a switch configuration in a multi-node processing system that directs transmission messages between nodes in order to balance the load of the network (Col. 26-27, lines 61-5; claim 25 – port-switching event is an unbalanced port-loading condition).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the process of Cam by considering an unbalanced port-loading condition as a port-switching event, as shown by Muller. This would further prevent any one port in Cam from consuming a disproportionate amount of bandwidth from the other ports and improve network utilization and efficiency.

Response to Arguments

6. Applicant's arguments filed 5/11/2006 have been fully considered but they are not persuasive.

- In the Remarks on pgs. 15-17 of the Amendment, Applicant contends that Bucholz does not disclose or suggest a data element that is indicative of the incomplete fragmentation status of a first available data packet, as recited in Applicant's claims. In particular, Applicant contends that none of the individual fields contained in the reassembly header 430 of Bucholz can be equivalent to the "data element" of the claims because they do not describe or make obvious a data element indicative of an incomplete fragmentation status.
- The Examiner respectfully disagrees. The Examiner is relying on Bucholz' disclosed reassembly header 430 *as a whole* (emphasis added) in meeting the claimed "data element". Applicant has argued how each individual field of Bucholz' header is not "indicative of the incomplete

fragmentation status of the first available packet", but has not considered how these fields, when taken together within the common header (data element), indicates the incomplete fragmentation status of the packet. In particular, the Total Fragment Field 640 and Fragment Number Field 650, when taken together, provide an indication of incomplete fragmentation status. For example, as a packet fragment is processed for transmission, if the Total Fragment Field 640 of the header attached to that packet fragment contains a value X while the Fragment Number Field 650 contains a value Y that is less than X, this provides an indication that the packet contains further data to be fragmented, thus meeting the contested claim limitations.

Conclusion

7. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gregory B. Sefcheck whose telephone number is 571-272-3098. The examiner can normally be reached on Monday-Friday, 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

GBS GBS
7-11-2006

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